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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,880	08/08/2005	Hans-Joachim Barth	10808/158	5306

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EXAMINER	
GOODWIN, DAVID J	

ART UNIT	PAPER NUMBER
2818	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/518,880	BARTH ET AL.	
	Examiner	Art Unit	
	DAVID GOODWIN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-32 and 34-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-32 and 34-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 25-28, 30, 31, 32, 34 –37, 39, 41-44, 47, 49, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (US 6,555,467) in view of Avanzino (US 2003/0218253)

3. Regarding claim 25.

4. Hsu teaches a semiconductor arrangement. Said arrangement comprises a substrate (12) (fig 1) (column 2 lines 20-30). A layer arranged on the substrate (12). The layer including a first subregion (18) and a second subregion (42, 72) arranged proximate the first subregion (18) (fig 7). The first subregion (18) being a decomposable material (column 2 lines 30-60) and the second subregion (42) having a structure of non-decomposable material (column 3 lines 10-40). A covering layer (82) positioned on the layer, including the first and second subregion (column 4 lines 55-65). An electrically conductive passiviation layer (40, 70) positioned between adjacent surface of the non-decomposable material and the covering layer (82) (fig 11) (column 4 lines 50-65). Wherein the decomposable material (18) is diffusible through the covering

layer (82) (fig 11,12) (column 5 lines 1-5). And the covering layer mechanically closes the first subregion off to the outside world.

5. Hsu does not teach the formation of an electrically conductive passivation layer substantially covering an upper surface of the structure of the non-decomposable material.

6. Avanzino teaches a process for forming a semiconductor layer arrangement. Said process comprises forming a non-decomposable material (54). And forming an electrically conductive passivation layer (55) substantially covering an upper surface of the structure of the non-decomposable material (54) (fig 14) (paragraph (0051).

7. It would have been obvious to form an electrically conductive passivation layer in order to prevent copper diffusion contamination of the surrounding dielectric

8. Regarding claim 26.

9. Hsu teaches an intermediate layer (16) between the substrate (12) and the layer of decomposable material (18) (fig 7) (column 2 lines 30-40).

10. Regarding claim 27.

11. Hsu teaches that the covering material (82) comprises a dielectric material (fig 11) (column 4 lines 55-65).

12. Regarding claim 28.

13. Hsu teaches that the covering layer comprises silicon oxide (column 4 lines 55-65).

14. Regarding claim 30.

15. Hsu teaches that the decomposable material (18) is diffusible through the covering layer (82) (fig 11,12) (column 5 lines 1-5).

16. Regarding claim 31.

17. Hsu teaches that the structure of the non-decomposable material (42, 72) is an electrically conductive material (column 3 lines 25-45).

18. Regarding claim 32

19. Hsu teaches that the structure of the non-decomposable material (42, 72) is copper (column 3 lines 25-45).

20. Regarding claim 34.

21. The nondecomposable structure comprises a dielectric material (80) (column 4 lines 50-60).

22. Regarding claim 35.

23. The nondecomposable structure comprises a silicon nitride (80) (column 4 lines 50-60).

24. Regarding claim 36.

25. Hsu teaches that the decomposable material (18) is thermally decomposable (column 5 lines 1-5).

26. Regarding claim 37.

27. Hsu teaches that the thermally decomposable material (18) is polynorborene (column 2 line 30-50).

28. Regarding claim 39.

29. At least one supporting structure (42, 72) is formed in the layer arranged between the substrate (12) and covering layer (82) (fig 11).

30. Regarding claim 41.

31. A protective passivation layer (40) at least partially surrounds the structure (fig 10).

32. Regarding claim 42.

33. Hsu teaches a method of making a semiconductor arrangement. Said method comprises a substrate (12) (fig 1) (column 2 lines 20-30). Forming a layer arranged on the substrate (12). The layer including a first subregion (18) and a second subregion (42, 72) arranged proximate the first subregion (18) (fig 7). The first subregion (18) being a decomposable material (column 2 lines 30-60) and the second subregion (42) having a structure of non-decomposable material (column 3 lines 10-40). Forming a covering layer (46, 82) positioned on the layer (column 4 lines 55-65). Forming an electrically conductive passiviation layer (40, 70) positioned between adjacent surfaces of the structure of the non-decomposable material and the covering layer (82) (fig 11) (column 4 lines 50-65). Wherein the decomposable material (18) is diffusible through the covering layer (82) the first subregion is mechanically closed off to the outside world (fig 11,12) (column 5 lines 1-5).

34. Hsu does not teach the formation of an electrically conductive passivation layer substantially covering an upper surface of the structure of the non-decomposable material.

35. Avanzino teaches a process for forming a semiconductor layer arrangement. Said process comprises forming a non-decomposable material (54). And forming an electrically conductive passivation layer (55) substantially covering an upper surface of the structure of the non-decomposable material (54) (fig 14) (paragraph (0051).

36. It would have been obvious to form an electrically conductive passivation layer in order to prevent copper diffusion contamination of the surrounding dielectric

37. Regarding claim 43.

38. Hsu teaches the decomposable material is encased in a casing comprising the substrate (12), the non-decomposable material (42, 72) and the covering material (82) (fig 10).

39. Regarding claim 44.

40. Hsu teaches that the decomposable material (18) is thermally decomposable (column 5 lines 1-5).

41. Regarding claim 47.

42. Hsu teaches depositing and patterning the decomposable material (18) on the substrate (12) (fig 6) (column 3 lines 10-30). Depositing (the material of the structure (42, 72) on the substrate (fig 7). Planarizing the surface of the deposited decomposable material and material of the structure (42) (fig 7) (column 3 lines 30-40).

43. Regarding claim 49.

44. Hsu teaches that at least one additional layer stack is formed on the covering layer(fig 11). The additional layer stack having an additional covering layer on an additional layer comprising decomposable material and a useful structure (fig 11, 12).

45. Regarding claim 50.

46. Hsu teaches that the structures that are separated by a covering layer (46) are coupled by at least one contact hole being introduced into the covering layer and being filled with electrically conductive material (fig 11).

47. Claims 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (US 6,555,467) in view of Avanzino (US 2003/0218253)as applied to claim 24 and further in view of Ibanbdeljalil (US 6,365,958).

48. Regarding claim 40.

49. Hsu in view of Avinzo teaches elements of the claimed invention above.

50. Hsu in view of Avinzo does not teach forming a protective structure along a lateral boundary of the substrate.

51. Ibanabdeljalil teaches forming protective structure (105) along a lateral boundary of a device having interconnect (104) thereon (fig 7a-7b) (column 11 lines 20-65).

52. It would have been obvious to put a protective structure taught by Ibanabdeljalil along the boundary of the substrate taught by Hsu in order to reduce the susceptibility to stress cracking of the device.

53. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (US 6,555,467) in view of Avanzino (US 2003/0218253) as applied to claim 24 and further in view of Brown (US 6,030,896).

54. Regarding claim 29.

55. Hsu in view of Avinzo teaches elements of the claimed invention above.

56. Hsu in view of Avinzo does not teach forming the structure on a silicon substrate.

57. Brown teaches forming an interconnect structure on a silicon substrate (column 4 lines 10-30).

58. It would have been obvious to one of ordinary skill in the art to form the structure on a silicon substrate so that active devices can be formed in the substrate and be connected to the interconnect.

59. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (US 6,555,467) in view of Avanzino (US 2003/0218253) as applied to claim 42 and further in view of Ito (US 6,573,607).

60. Regarding claim 46

61. Hsu in view of Avanzino (US 2003/0218253) teaches elements of the claimed invention above.

62. Hsu in view of Avanzino (US 2003/0218253) does not teach forming the barrier layer by CVD.

63. Ito teaches forming a metal barrier layer for copper interconnect by CVD deposition of tantalum (column 4 lines 10-25).

64. It would have been obvious to one of ordinary skill in the art to form a barrier layer for a copper interconnect structure by CVD in order to form a highly conformal layer which will prevent copper out diffusion.

65. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (US 6,555,467) in view of Avanzino (US 2003/0218253) as applied to claim 42 and further in view of Brown (US 6,030,896).

66. Regarding claim 48.

67. Hsu in view of Avanzino (US 2003/0218253) teaches elements of the claimed invention above.

68. Hsu in view of Avanzino (US 2003/0218253) does not teach depositing and patterning the structure material and then planarizing the surface.

69. Brown teaches a method of making a device. Said method comprises depositing a conductive material (18) (fig 1) and then patterning said material (fig 2) (column 4 lines 20-50). A dielectric (24) is then formed between the lines of conductive material and planarized (fig 4) (column 5 lines 5-20).

70. It would have been obvious tone of ordinary skill in the art to pattern the metal layer prior to the deposition of the dielectric in order to reduce the chance of copper contamination and to prevent reduce to the underlying patterns.

71. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (US 6,555,467) in view of Avanzino (US 2003/0218253) as applied to claim 24 and further in view of Kohl (US 2002/0081787).

72. Regarding claim 38.

73. Hsu in view of Avanzino (US 2003/0218253) teaches elements of the claimed invention above.

74. Hsu in view of Avanzino (US 2003/0218253) does not teach that the decomposable material may be photosensitive.

75. Kohl teaches the use of a photosensitive decomposable material in the formation interconnect dielectric (paragraph 0080).

76. It would have been obvious to one of ordinary skill in the art to make the decomposable material photosensitive in so that less thermal energy is required to decompose the material.

77. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (US 6,555,467) in view of Avanzino (US 2003/0218253) as applied to claim 42 and further in view of Leu (US 6,605,874).

78. Regarding claim 45.

79. Hsu in view of Avanzino (US 2003/0218253) teaches elements of the claimed invention above.

80. Hsu teaches that the structure of the non-decomposable material (42, 72) is copper (column 3 lines 25-45).

81. Hsu in view of Avanzino (US 2003/0218253) does not teach that a barrier layer comprises cobalt phosphorous.

82. Leu teaches forming a barrier layer (118) on interconnect by electroless deposition (column 13 lines 10-18)

83. It would have been obvious to one of ordinary skill in the art to form a cobalt phosphorous barrier layer in order to prevent copper diffusion.

Response to Arguments

84. Applicant's arguments with respect to claims 25-32, 34 through 50 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID GOODWIN whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJG

/Steven Loke/
Supervisory Patent Examiner, Art Unit 2818